CLAIMS

1. (Currently Amended) A microprocessor configured for executing at least one instruction, the microprocessor having a main processor clock, the microprocessor comprising:

a first stage having one or more storage components configured for storing operand data of the at least one instruction, the first stage being clocked by at least a first clock derived from the main processor clock;

a first combinatorial logic connected to the first stage for receiving the operand data from the first stage and configured for processing the operand data and generating first output data, wherein the first clock is operational only during a first period of time when the operand data is processed by the first combinatorial logic;

a second stage of one or more storage components configured for storing the first output data, the second stage being clocked by at least a second clock derived from the main processor clock;

control logic that is at least configured to:

generate at least one instruction-valid control bit, wherein the at least one instruction-valid control bit is configured to selectively disable ~~only~~ the first clock derived from the main processor clock if a first stage is unused or to disable ~~only~~ the second clock derived from the main processor clock if a second stage is unused, and wherein the at least one instruction-valid control bit is configured to enable the first clock and the second clock in response to a scan mode signal; and

a second combinatorial logic connected to the second stage for receiving the first output data from the second stage and configured for processing the first output data and generating second

output data, wherein the second clock is operational only during a second period of time when the first output data is processed by the second combinatorial logic.

2. (Original) The microprocessor of Claim 1, further comprising:

a first local clock buffer connected to the first stage for providing at least the first clock to the first stage only during the first period of time;

a second local clock buffer configured for generating the second clock and connected to the second stage for providing at least the second clock to the second stage only during the second period of time.

3. (Original) The microprocessor of Claim 1, further comprising:

a first local clock buffer connected to the first stage for providing at least the first clock to the first stage only during the first period of time;

a second local clock buffer configured for generating the second clock and connected to the second stage for providing at least the second clock to the second stage only during the second period of time; and

a dynamic clock-control unit connected to at least the first local clock buffer for providing a first control signal to at least the first local clock buffer and configured for generating the first control signal, the first control signal enabling the first clock signal to be operational only during the first period of time.

4. (Original) The microprocessor of Claim 1, further comprising an integrated storage component configured for storing the operand data, the integrated storage component being

connected to the first stage for providing the operand data to the first stage and being connected to the second combinatorial logic for receiving the second output data from the second combinatorial logic.

5. (Original) The microprocessor of Claim 1, further comprising:

an integrated storage component configured for storing the operand data, the integrated storage component being connected to the first stage for providing the operand data to the first stage and being connected to the second combinatorial logic for receiving the second output data from the second combinatorial logic;

a first local clock buffer connected to the first stage for providing at least the first clock to the first stage only during the first period of time; and

a second local clock buffer configured for generating the second clock and connected to the second stage for providing at least the second clock to the second stage only during the second period of time.

6. (Original) The microprocessor of Claim 1, wherein the first stage comprises one or more latches, and wherein the second stage comprises one or more latches.

7. (Original) The microprocessor of Claim 1, further comprising an integrated storage component configured for storing the operand data, the integrated storage component being connected to the first stage for providing the operand data to the first stage and being connected to the second combinatorial logic for receiving the second output data from the second combinatorial logic, wherein the integrated storage component comprises an array.

8. (Original) The microprocessor of Claim 1, wherein the second period of time is automatically determined by delaying the first period of time by one cycle of the main processor clock.

9. (Original) The microprocessor of Claim 1, further comprising:

an integrated storage component configured for storing the operand data, the integrated storage component being connected to the first stage for providing the operand data to the first stage and being connected to the second combinatorial logic for receiving the second output data from the second combinatorial logic;

a first local clock buffer connected to the first stage for providing at least the first clock to the first stage only during the first period of time;

a second local clock buffer configured for generating the second clock and connected to the second stage for providing at least the second clock to the second stage only during the second period of time; and

a dynamic clock-control unit connected to at least the first local clock buffer for providing a first control signal to at least the first local clock buffer and configured for generating the first control signal, the first control signal enabling the first clock signal to be operational only during the first period of time.

10. (Original) The microprocessor of Claim 1, wherein each storage component in the first stage comprises:

a master latch configured for storing the operand data and being clocked by a first master clock derived from the first clock; and

a slave latch connected to the master latch for receiving the operand data from the master latch and storing the operand data, the slave latch being configured for being clocked by a first slave clock derived from the first clock.

11. (Currently Amended) A method for dynamically reducing power consumption in a microprocessor configured for executing at least an instruction, the microprocessor having a main processor clock, the method comprising the steps of:

storing operand data in a first stage of one or more storage components residing in the microprocessor, the first stage being clocked by at least a first clock derived from the main processor clock;

transmitting the operand data from the first stage to a first combinatorial logic residing in the microprocessor, wherein the first clock is operational only during a first period of time when the operand data is processed by the first combinatorial logic;

processing the operand data in the first combinatorial logic;

generating first output data from the first combinatorial logic;

storing the first output data in a second stage of one or more storage components residing in the microprocessor, the second stage being clocked by at least a second clock derived from the main processor clock;

transmitting the first output data from the second stage to a second combinatorial logic residing in the microprocessor, wherein the second clock is operational only during a second period of time when the first output data is processed by the second combinatorial logic;

processing the first output data in the second combinatorial logic;

generating second output data from the second combinatorial logic;

generating an instruction-valid control bit;

in response to the instruction-valid control bit, reducing power consumption in the microprocessor by dynamically controlling the first and second clocks by selectively disabling at least one local clock buffer to prevent switching of ~~only~~ the first clock or ~~only~~ the second clock;

generating a scan mode signal, wherein in response to the scan mode signal, the instruction-valid control bit enables the first clock and the second clock.

12. (Original) The method of Claim 11, further comprising the steps of:

transmitting at least the first clock from a first local clock buffer to the first stage only during the first period of time;

generating the second clock from a second local clock buffer; and

transmitting at least the second clock from the second local clock buffer to the second stage only during the second period of time.

13. (Original) The method of Claim 11, further comprising the steps of:

transmitting at least the first clock from a first local clock buffer to the first stage only during the first period of time;

generating the second clock by a second local clock buffer;

transmitting at least the second clock from the second local clock buffer to the second stage only during the second period of time.

generating a first control signal;

transmitting the first control signal from the dynamic clock-control unit to at least the first local clock buffer; and

enabling the first clock signal by the first control signal to be operational only during the first period of time.

14. (Original) The method of Claim 11, further comprising the steps of:

storing the operand data in an integrated storage component residing in the microprocessor;

transmitting the operand data from the integrated storage component to the first stage; and

transmitting the second output data from the second combinatorial logic to the integrated storage component.

15. (Original) The method of Claim 11, further comprising the steps of:

transmitting at least the first clock from a first local clock buffer to the first stage only during the first period of time;

generating the second clock from a second local clock buffer;

transmitting at least the second clock from the second local clock buffer to the second stage only during the second period of time;

storing the operand data in an integrated storage component residing in the microprocessor;

transmitting the operand data from the integrated storage component to the first stage; and

transmitting the second output data from the second combinatorial logic to the integrated storage component.

16. (Original) The method of Claim 11, further comprising the steps of:

transmitting at least the first clock from a first local clock buffer to the first stage only during the first period of time;

generating the second clock from a second local clock buffer;

transmitting at least the second clock from the second local clock buffer to the second stage only during the second period of time.

generating a first control signal by a dynamic clock-control unit residing in the microprocessor;

transmitting the first control signal from the dynamic clock-control unit to at least the first local clock buffer;

using the first control signal to enable the first clock signal to be operational only during the first period of time;

storing the operand data in an integrated storage component residing in the microprocessor;

transmitting the operand data from the integrated storage component to the first stage; and

transmitting the second output data from the second combinatorial logic to the integrated storage component.

17. (Currently Amended) A method for dynamic power management in an execution unit using pipeline wave flow control having multiple stages with clocks interconnected thereto comprising:

storing operand data in a first stage of one or more storage components residing in the execution unit;

transmitting the operand data from the first stage to a first combinatorial logic residing in the execution unit, wherein the clock of the first stage is operational only during a first period of time when the operand data is processed by the first combinatorial logic;

processing the operand data in the first combinatorial logic;

generating first output data from the first combinatorial logic;

storing the first output data in a second stage of one or more storage components residing in the execution pipeline;

transmitting the first output data from the second stage to a second combinatorial logic residing in the execution unit, wherein the clock of the second stage is operational only during a second period of time when the first output data is processed by the second combinatorial logic;

processing the first output data in the second combinatorial logic;

generating second output data from the second combinatorial logic;

generating an instruction-valid control bit;

in response to the instruction-valid control bit, reducing power consumption in the execution unit by dynamically controlling the first and second clocks by selectively disabling at least one local clock buffer to prevent switching of ~~only~~ the first clock or ~~only~~ the second clock;

generating a scan mode signal, wherein in response to the scan mode signal, the instruction-valid control bit enables the first clock and the second clock.

18. (Currently Amended) A microprocessor configured for executing at least one instruction, the microprocessor having a main processor clock, the microprocessor comprising:

a first stage having one or more storage components configured for storing operand data of the at least one instruction, the first stage being clocked by at least a first clock derived from the main processor clock;

a first combinatorial logic connected to the first stage for receiving the operand data from the first stage and configured for processing the operand data and generating first output data,

wherein the first clock is operational only during a first period of time when the operand data is processed by the first combinatorial logic;

a second stage of one or more storage components configured for storing the first output data, the second stage being clocked by at least a second clock derived from the main processor clock;

control logic that is at least configured to:

generate at least two instruction-valid control bits, wherein the at least two instruction-valid control bits are configured to:

disable the first clock derived from the main processor clock by a first instruction-valid control bit if a first stage is unused or ~~to~~ disable the second clock derived from the main processor clock by a second instruction-valid control bit if a second stage is unused;

enable the first clock and the second clock in response to a scan mode signal;

disable the first clock by the first instruction-valid control bit in response to a first stop control signal and disable the second clock by the second instruction-valid control bit in response to a second stop control signal; and

a second combinatorial logic connected to the second stage for receiving the first output data from the second stage and configured for processing the first output data and generating second output data, wherein the second clock is operational only during a second period of time when the first output data is processed by the second combinatorial logic.